ABSTRACT

Disclosed herein is a method of forming a floating gate in a non-volatile memory device having a self-aligned shallow trench isolation (SA-STI) structure. First, a tunnel oxide layer is formed on a semiconductor substrate having a SA-STI structure. Next, a first floating gate layer is formed on the tunnel oxide layer at a first temperature of no less than about 530°C. A second floating gate layer is then formed on the first floating gate layer at a second temperature of no more than 580°C. After depositing the first floating gate layer, the second floating gate layer is in-situ deposited to prevent the growth of a native oxide layer on the surface of the first floating gate layer. Thus, gate resistance can be reduced and process time can be shortened.